# A Comparative Study of Heavy-Ion and Proton-Induced Bit-Error Sensitivity and Complex Burst-Error Modes in Commercially Available High-Speed SiGe BiCMOS

Paul Marshall, *Member, IEEE*, Marty Carts, *Member, IEEE*, Art Campbell, *Senior Member, IEEE*, Ray Ladbury, *Member, IEEE*, Robert Reed, *Member, IEEE*, Cheryl Marshall, Steve Currie, Dale McMorrow, Steve Buchner, *Member, IEEE*, Christina Seidleck, Pam Riggs, Karl Fritz, Barb Randall, and Barry Gilbert, *Fellow, IEEE*

***Abstract*—We compare heavy ion and proton SEE data on commercial SiGe technologies from IBMs 7 HP and 5 AM processes and Jazz Semiconductors SiGe120 process at data rates from 50 Mb/s to 12.4 Gb/s. Complex burst-error trends correlate with both data rate and particle LET, as well as pulsed laser probing of both data paths and clock distribution circuitry.**

***Index Terms*—Ground testing, high-speed testing, silicon germanium (SiGe), single-event effect (SEE), single-event upset (SEU).**

## I. Introduction

In previous years, we and other authors, have conducted several investigations showing very encouraging total ionizing dose (TID) results in the 1st and second generations of IBMs SiGe BiCMOS processes (known as 5 HP and 7 HP) ([1] and references therein). However, over recent years the demonstration of sensitivity to single event effects has arisen as a key concern for some applications [2]–[8]. These concerns were first demonstrated experimentally in [2] in the 5 HP version of the process with half-micron drawn feature sizes, and more recently in IBMs 7 HP SiGe BiCMOS [3], which included charge collection and modeling results implying that the electrically active substrate was an important factor. Additional modeling studies and an increasing understanding of the role of the substrate are expanded on in [4]–[8]. To date, there has not been a successful demonstration of SEE hardening in SiGe, but the technology continues to advance and grow in importance to the satellite community.

Our study has three primary contributions to furthering the understanding of commercially available SiGe technology. First, we step back from the high speed HBT oriented investigations covered in [1]–[8] to look carefully at the CMOS used in IBMs 5 HP SiGe BiCMOS product family. To date, these are the first investigations to report on the latch-up and SEU characteristics of this key aspect of 5 HP SiGe BiCMOS. Next, we provide a detailed comparison of IBMs 7 HP SiGe HBT logic with its commercially competitive counterpart from Jazz Semiconductor. For this comparison, identical 127-b shift register circuits have been fabricated and tested to the same heavy ion and proton environments using exactly the same test equipment for both tests. The remainder of this paper will provide highlights of these studies, and also introduce new data providing insights into the evolution of complex error signatures that appear to be common to both families of high speed SiGe.

## II. Test Structures and Experimental Setup

The IBM 7 HP SiGe HBT process and ion-induced charge collection characteristics have been previously described [3], The process uses a 0.18-$\mu$m minimum feature size SiGe HBT resulting in a fT of 120 GHz. The Jazz SiGe120 HBT also uses both deep and shallow trench isolation with the same minimum feature size, but with a slightly higher fT of 155 GHz. The CMOS devices were designed in IBMs 5 AM CMOS process as part of a multiproject wafer fabrication. The test vehicle was processed at IBMs commercial facilities in Burlington, VT, and our design was incorporated into a multiuser mask set through

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P. Marshall is a consultant and is at Brookneal, VA 24528 USA (e-mail: PWMarshall@aol.com).

M. Carts and C. Seidleck are with Raytheon Information Technology, Lanham, MD 20706 USA.

A. Campbell and D. McMorrow are with the Naval Research Laboratory, Washington, DC 20375 USA.

R. Ladbury is with Orbital Sciences Corporation, McLean, VA 20166 USA.

R. Reed was with NASA/GSFC, Code 561.4, Greenbelt, MD 20771 USA, and is now with Vanderbilt University, Nashville, TN 37235 USA.

C. Marshall is with NASA/GSFC, Code 561.4, Greenbelt, MD 20771 USA.

S. Currie, P. Riggs, K. Fritz, B. Randall, and B. Gilbert are with The Mayo Foundation, Rochester, MN 55905 USA.

S. Buchner is with QSS Group, Inc., Greenbelt, MD 20771 USA.

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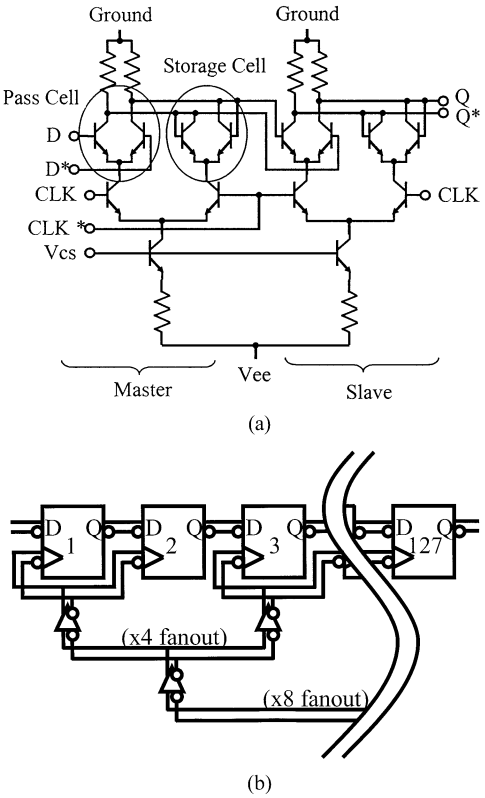


Fig. 1. (a) Standard master-slave architecture was used for the 127-b-long serial shift register depicted in (b). This example from the IBM 7 HP design shows a master clock fan-out followed a 64, 32, 8, and 4 node architecture.

the services of MOSIS.[1] The process version available through MOSIS is known as 5 AM, and differs only in the details of the top level metal from the 5 HP commercial CMOS process. The 5 AM process uses a 0.5 $\mu$m drawn minimum feature size.

Similar SiGe test articles for both the IBM and Jazz processes were designed and packaged by the Mayo Foundation. The test articles were both digital serial shift registers using a standard master-slave flip-flop as indicated in Fig. 1(a) and configured as a 127-b-long serial shift register as indicated in Fig. 1(b). The current mode logic (CML) DUT interfaces include differential data inputs and outputs, as well as differential clock inputs. In the case of the IBM deivce, the single master clock input is fanned out to 64, 32, 8, and at the lowest level four register stages. Similarly, master clock fanout on the Jazz SiGe120 device was at levels of 80, 20, and 5 registers. The 5 AM CMOS DUT is also designed as a 127-b-long serial shift register, but with CMOS LVDS I/O.

The test set used for both SiGe DUT types is shown as Fig. 2. We used a 7-b linear feedback shift register to provide a 127-b pseudorandom sequence (described in [2]) for differential data inputs to the DUT. The commercially available Anritsu pattern detector was programmed to recognize the expected 127-b sequence, and provide full error reporting, including the number of errors per error event and their positions in the bit stream. The GPIB interface to the Anritsu BERT captured a 256-b pattern centered on the bit error triggering the event so that full pattern reconstruction was possible, and all bits deviating

[1]Available: http://www.mosis.org/Products/menu-products.html.

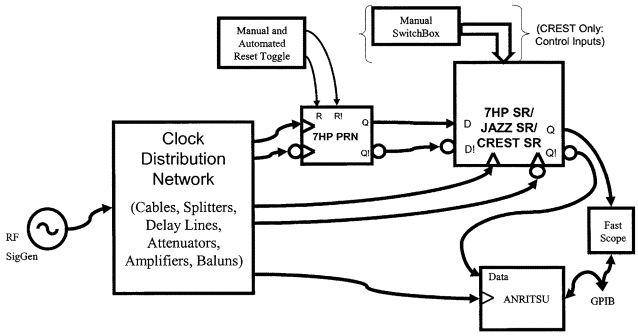


Fig. 2. Anritsu commercial BERT detector received the data stream from the IBM 7 HP HBT DUT and captured errors at data rates from 50 Mb/s to 12.4 Gb/s. A 7 HP PRN data source supplied the IBM and Jazz setups.

from the expected pattern were identified in post-processing. The upper bandwidth limit of this unit at 12.4 Gb/s limited the test capability for both the IBM and Jazz DUT types, and fast sampling scope eye diagrams suggested the devices would perform to $>$16 Gb/s. The 5 AM CMOS register was tested in a similar configuration, but with a commercial bit-error rate test (BERT) set manufactured by Broadband Communications Products (BCP Model 110/210). The CMOS register operates to $\sim$700 Mb/s, and this was well within the 1 Gb/s limit of the BCP test equipment.

All heavy ion tests were performed at the Texas A&M cyclotron facility. For the IBM and Jazz HBT devices, Ne, Ar, Kr, and Xe tunes at 15 MeV/amu were used, and for the IBM 5 AM CMOS register, the same ions were used but with a 25 MeV/amu tune. Proton tests were performed at the University of California Davis Crocker Nuclear Laboratory with cyclotron tunes at 63 and 28 MeV. Two examples of each DUT type were tested over the range of data rates at LETs of 2.8 and 53 MeV $\cdot$ cm$^2$/mg, and no statistically significant part-to-part variation in event cross section was detectable.

Pulsed laser tests were performed at the NRL laser test facility [9]. The laser-induced charge collection measurements were performed with nominally 1 ps duration optical pulses centered at 590 nm (2.1 eV). The laser pulse repetition rate was varied between 10 Hz and 1 kHz, depending on the particular test performed. The optical pulses were focused onto the device under test (DUT) with a 100$\times$ microscope objective, resulting in a Gaussian spot size of 1.2 $\mu$m at the surface of the DUT. The $1/\mathrm{e}$ optical penetration depth in silicon at 590 nm wavelength is approximately 1.8 $\mu$m. The DUT was mounted on a motorized $xyz$ stage with 0.1 $\mu$m resolution, and the laser-induced SEU thresholds were determined for each node of interest by optimizing the $x-y$ position and focus to obtain the minimum laser pulse energy able to induce an upset. The pulse energy was monitored with a calibrated large-area photodiode, and the incident pulse energy was converted into deposited charge by correcting for reflection losses and assuming that each photon gives rise to a single electron–hole pair.

## III. See Results for IBM and Jazz HBT Circuits

Fig. 3 parts a and b compare the heavy ion device level error event cross sections for the IBM 7 HP HBT register with those measured on the Jazz device. For this plot we have chosen

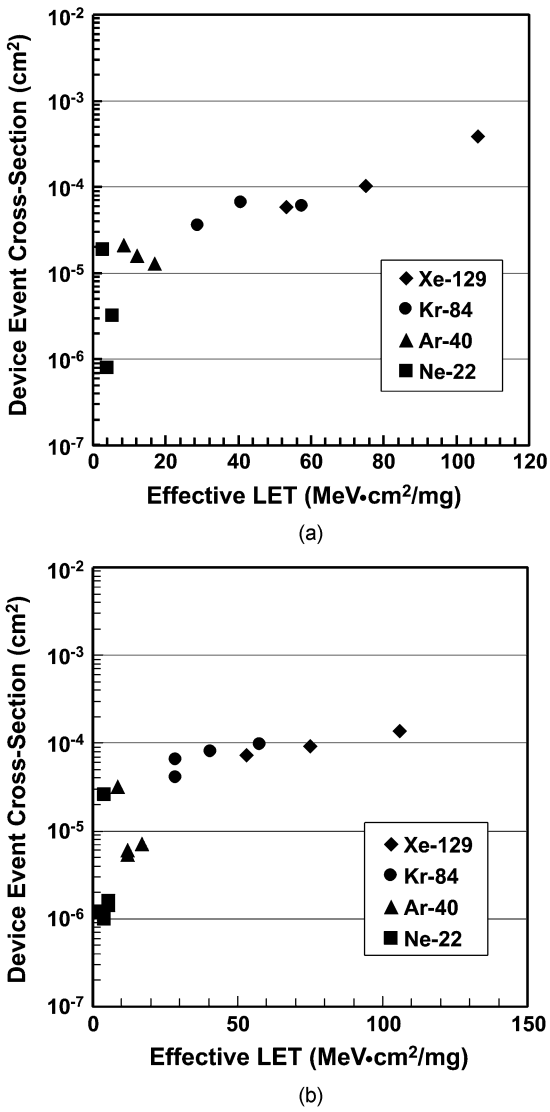


Fig. 3. (a) Even at 50 Mb/s, the 7 HP 127-b serial register showed a large high-LET cross section as well as a low threshold LET, indicating a definite sensitivity to soft errors. (b) Jazz SiGe120 shows a similar response, and in both cases the cross section is per event. Many events involved more than one bit in error.

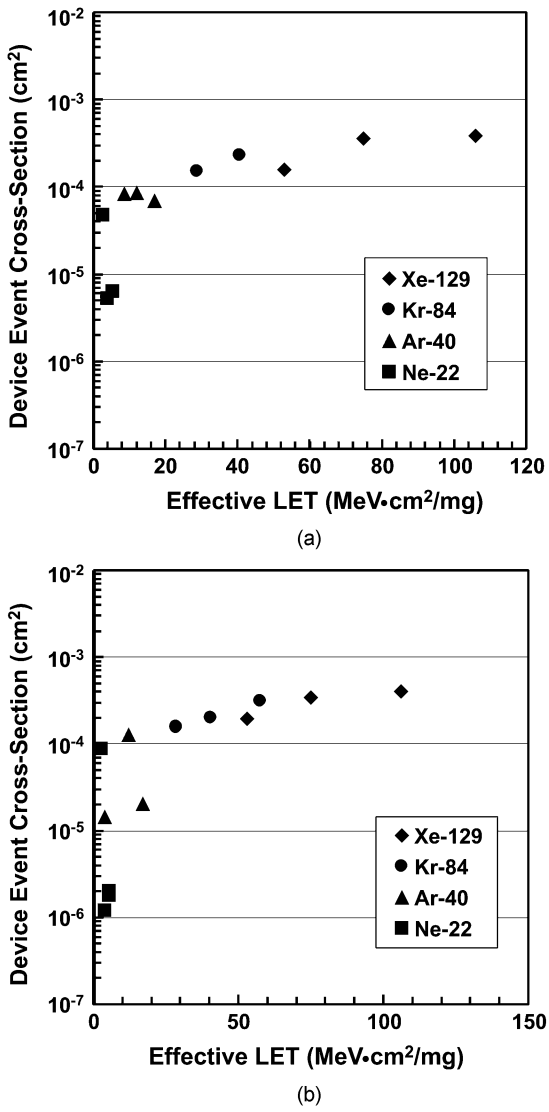


Fig. 4. (a) IBM 7 HP and (b) Jazz SiGe120 show that at 12.4 Gb/s the event cross sections for both technologies have increased significantly, and are remarkably similar. For the 127 stage register, these data indicate sensitive areas exceeding 300 $\mu$m$^2$ per D-flip-flop stage.

the event, rather than the error cross section, and note that all events are counted equally regardless of the duration of the error. Results in both technologies are characterized by both a low threshold LET and a large cross section at high LETs. The high LET device cross section of $\sim 10^{-4}$ cm$^2$ corresponds to a sensitive area of $\sim$80 $\mu$m$^2$ per D-flip-flop stage, and we note the results described in [3] indicating charge collection by diffusion from beyond the deep trench boundaries. We also note the unexpected trend of decreasing cross section with increasing incidence angle at low LETs which has also been reported in other 5 HP and 7 HP circuits [2] and [3]. Data were acquired at each LET for at least seven data rates covering the range from 50 Mb/s to 12.4 Gb/s. Results presented in Fig. 4(a) and (b) measured at 12.4 Gb/s, the upper limit of our test equipment, indicate a factor of $\sim$5 increase in saturated event cross section over this data rate range covering over two orders of magnitude. The associated inferred sensitive area per D-flip-flop exceeds 300 $\mu$m$^2$ at 12.4 Gb/s.

The event cross section increases with frequency only near the lower end of the data rate range as indicated in Fig. 5(a) and (b), and there is a remarkable lack of dependence on the event cross section with data rate in the upper end of this range. A number of previous studies (e.g., [2], [10], [11], and references therein) have noted, in some cases, an increasing error cross section with increasing data rate and explained this in terms of the "window of vulnerability," presumably associated with increased sensitivity to SEE during clock edge transitions. We note that at lower data rates, corresponding to bit periods of less than 1–2 ns, we see such an increase, and this is consistent with the clock edge related sensitivity. However, at higher data rates, the data indicate saturation in the temporal domain, and further increases in the event cross section should not be expected.

We note however, that the event cross section tells only a portion of the story. In Fig. 6(a) and (b) we examine the average errors per error event as it trends with data rate at five different

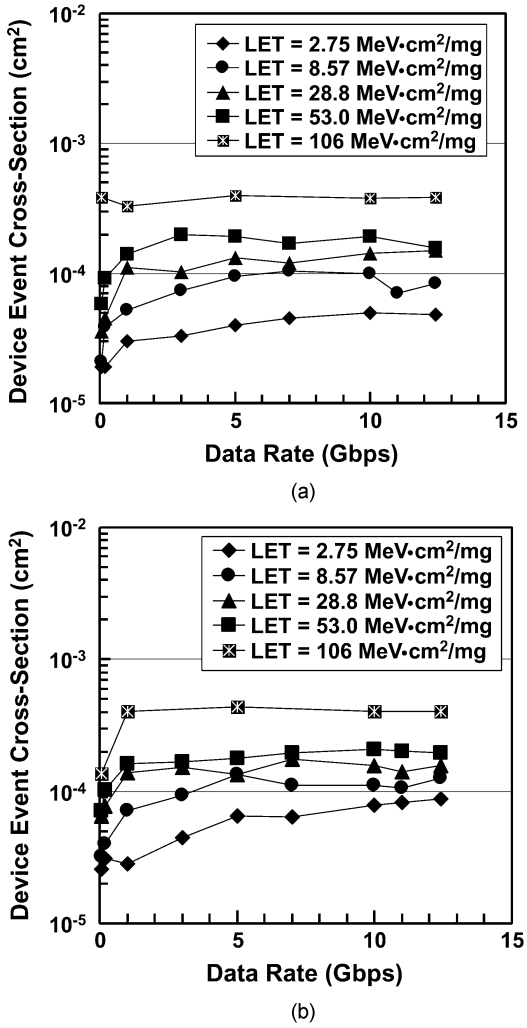


Fig. 5. (a) For the IBM 7 HP and (b) for the Jazz SiGe120 show a similar and remarkably weak trend of event cross section with data rate. The flatness at high LETs above ~1 Gb/s is interpreted as saturation in both the spatial and temporal domains.

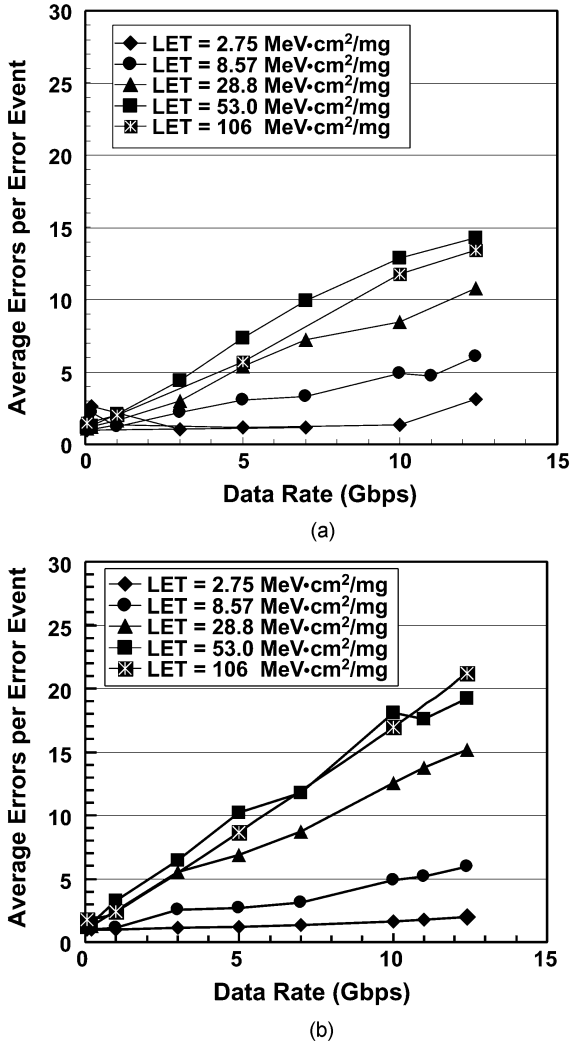


Fig. 6. (a) For both the IBM 7 HP and (b) Jazz SiGe120 register, the average number of errors per error event tended up with both data rate and with particle LET. As the text explains, this is a useful, but incomplete description of error bursts.

LETs. Clearly, at the lower data rates, most errors are only single bit errors even at high LETs. But, there is a strong trend toward longer error bursts when an event corresponds to a high data rate. This is especially so with high LET particles. In terms of the "window of vulnerability" argument, for bit periods shorter than about 1 ns, multiple clock edges or "windows" are affected by a single event, hence leading to multiple bit errors. This description is completely consistent with the measurement and simulation studies reported in [3], [4], [6], and [8]] which describe the charge collection transient as having a $1/e$ time constant on the order of 2 ns. It is quite remarkable that in both the IBM and Jazz circuits, when bit periods of 100 ps are considered, the average number of bits in error is just over 10, again corresponding well with the ~1 ns error event duration.

Proton testing of the IBM 7 HP circuit at energies of 28 and 63 MeV were dominated by single bit errors. The 50 Mb/s device event cross sections were $2 \times 10^{-11}$ cm$^2$ and $5 \times 10^{-11}$ cm$^2$ respectively. At 5 Gb/s, these had increased to $5 \times 10^{-11}$ cm$^2$ and $7 \times 10^{-11}$ cm$^2$, and by 12.4 Gb/s they were both at $1 \times 10^{-10}$ cm$^2$.

## IV. Burst-Error Characteristics

While the description in terms of event cross section coupled with average errors per event is informative, it still tells only a portion of the story. We note similarity between the IBM and Jazz devices, and in Fig. 7 show only the IBM result plotted as a histogram showing the number of bits in error at two LETs measured at 12.4 Gb/s. Clearly, an average number of errors, even with statistical uncertainty, is an inadequate picture. This relation strongly suggests that the charge collection process involves 3-D geometries and the conventional assumptions associated with rectangular parallel-piped geometry are not applicable. Also, we see from Fig. 7 that the "typical" number of bits in error tends toward higher numbers with the higher LET, and lower numbers of bit errors become less frequent, but there is obviously more going on than fixed temporal outages associated with individual register stages.

Using the NRL pulsed laser test facility, we conducted a detailed study of various potential error targets and error modes, again with similar findings for the IBM and Jazz circuits. To understand these results, consider the cartoon depiction of error

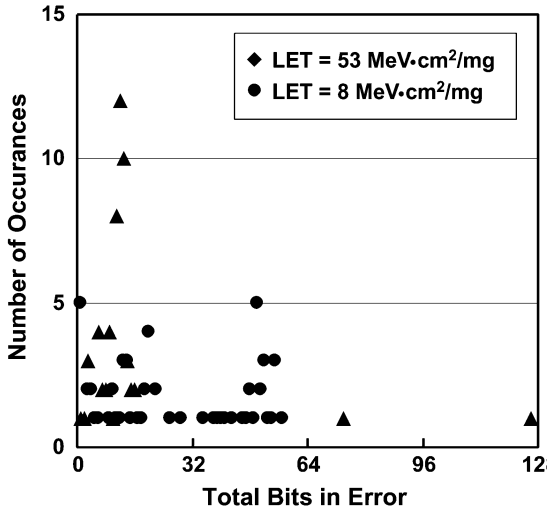


Fig. 7. For the IBM 7 HP register operated at 12.4 Gb/s, this histogram shows how the total bits in error increases with LET, but less frequent large error bursts are still seen at the lower LET.

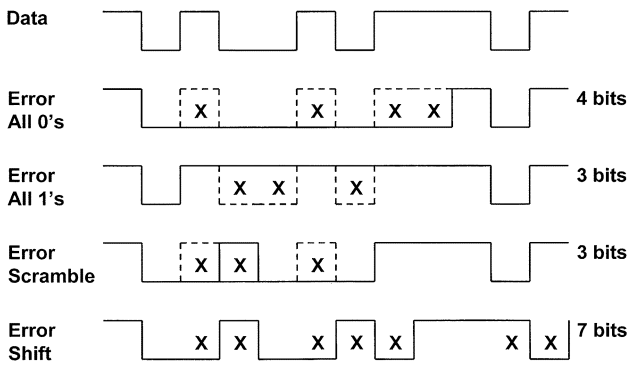


Fig. 8. In this cartoon, four categories of multiple bit errors are compared with the expected data stream. Pattern shifts appear to be due to either extra or suppressed clock edges.

types shown as Fig. 8. First, given the nature of the pseudo-random $(2^7 - 1)$ data sequence, an event which disrupts the circuit and induces an arbitrary state has a 50% chance of inducing an error condition for that bit period. Consequently, we have to look across multiple bit intervals and group events that are within close proximity. We considered errors within 8-b periods to meet this criterion, and this selection was based on analysis of many error histories that showed multiple bit-error events did not contain error free intervals of as many as 8 b.

Metallization coverage of the top side of the circuit prevented highly quantitative correlations between heavy ion LET and laser pulse energy, but relative trends were very apparent. We found that at low laser pulse energy, the data registers were most sensitive and single bit errors could follow from hits to either the pass or storage transistors [see Fig. 1(a)]. With higher pulse energy, hits to these HBTs could result in temporal disturbances lasting for multiple bit periods; typically forcing either "all ones," or if the complementary transistor were hit, "all zeros." The current source transistors exhibited less sensitivity, as did the data register clock input transistors, and hits to these regions typically induced either single bit errors or "mangles" covering multiple (but not always contiguous) bits.

As previously mentioned, the single master clock fan-out levels covered 64, 32, 8, or 4 register stages, and we saw clear correlations with sensitivity in these targets in terms of error length and the ability to realign to recover the pattern thus indicating a "shift" error. We noted "shift" errors both forward and backward in the data sequence and interpret these as either extra clock edges or suppressed clock edges. It is also noteworthy that hits to a given node in the clock tree could affect more bits than its fan-out would suggest by one level, e.g., hits to the $\times 32$ node could affect up to 64 bits. This is strong evidence of the role of single event transients in the propagation of errors, which is expected based on previous studies of the 5 HP HBT logic family [2].

Using insights gained from the pulsed laser ion testing, heavy ion data were analyzed to determine whether upsets—particularly multibit upsets—could be grouped into categories that might give clues as to the portions of the microcircuit that were upsetting. Because the device geometry gives rise to a SEE response as a function of ion incident angle, only data for normally incident ions were considered. Upset lengths were defined as the number of affected bits from the first bit in error until the first bit where the correct pattern was resumed (as indicated by transmission of a fully correct 7-b sequence). These upset lengths were then plotted for each run. Laborious examination of the upsets revealed several types of errors. Aside from single bit errors, we identified errors as being either "all zeros," "all ones," "mangles" (a mixture of zeros and ones) and "shifts." Typically, the "shift" error was characterized as one that could be restored to the expected bit sequence by either shifting forward or backward in time by one or two bit periods.

Cross sections were calculated for single bit errors and for each multibit error type, and histograms upset length were constructed for the single bit errors, "all zeros," all ones, "mangle errors," and "shift errors." These data were analyzed for trends with LET and operating frequency. We found that the sensitivity in the data registers dominated, and noted primarily single bit hits or bursts of ones, zeros, or to a lesser extent, "mangles." Long bursts of "mangles," or "shift" errors were correlated with clock tree hits.

Fig. 9(a) and (b) compare heavy ion data on the IBM 7 HP register and show the device event cross sections decomposed into the various error categories just described. Based on the pulsed laser study interpretation, we see no surprises here. Data of Fig. 9(a), showing the error type data rate dependence at a lower LET, indicate primarily single bit errors giving way to multiple bit bursts of zeros and ones at higher data rates. "Shift" errors were noted, but at a lower level, and this is consistent with the two isolated long bursts shown for an LET of 8 MeV $\cdot$ cm$^2$/mg in Fig. 7. Fig. 9(b), at the higher LET reveals a much richer mix of burst-error characteristics at the higher data rates.

Pulsed laser testing and heavy ion results for the Jazz SiGe120 circuit show strikingly similar behavior, but with a slightly higher occurrence of longer error bursts at high speed and LET [see Fig. 6(b)]. We believe these are the first data reported which describe this complex error behavior, and it obviously has consequences for error correcting algorithms.

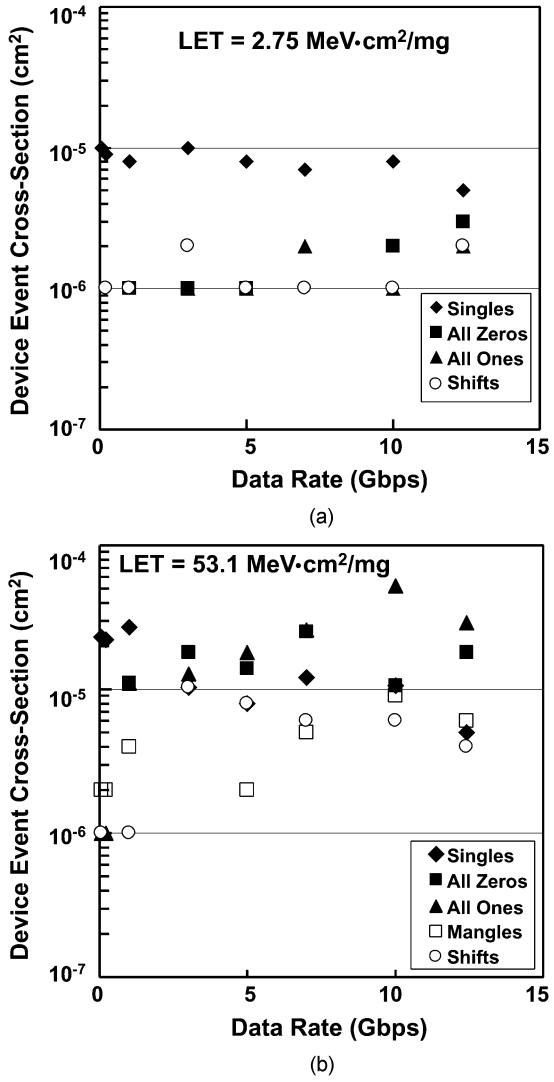


Fig. 9. (a)–(b) The two charts compare the IBM 7 HP cross sections for single and complex error bursts at low and high LET. The low LET shows an increasing trend to multiple event errors at higher speeds, and the higher LET shows a mix of various error types. No "mangle" errors were seen at the lower LET.

## V. See Performance of 5 AM CMOS

A 5 AM CMOS 127 bit serial shift register was also designed using a standard master-slave flip-flop architecture. The test set similar to the one shown as Fig. 2 incorporated a commercial BERT which operates from 7 Mb/s to 1 Gb/s. Amplifiers and bias tees converted the CML levels from the BERT pattern generator to proper CMOS LVDS levels to drive the differential data and differential clock inputs of the CMOS DUT. In the absence of particles, the circuit operated error free under broadband conditions from 10 to 670 Mb/s. This upper limit was common to the three CMOS DUTs we examined, and closely matches the limiting data rate expected from SPICE circuit simulations.

One significant motivation for this test concerned the possibility of single event latch-up (SEL). No evidence of any form of latch-up was seen, even after fluences exceeding $10^8$ ions/cm$^2$ of Xe with LET $>53$ MeV $\cdot$ cm$^2$/mg.

Bit-error events are seen, and the data of Fig. 10 show an onset threshold LET of 18 MeV·cm$^2$/mg with a saturated device event

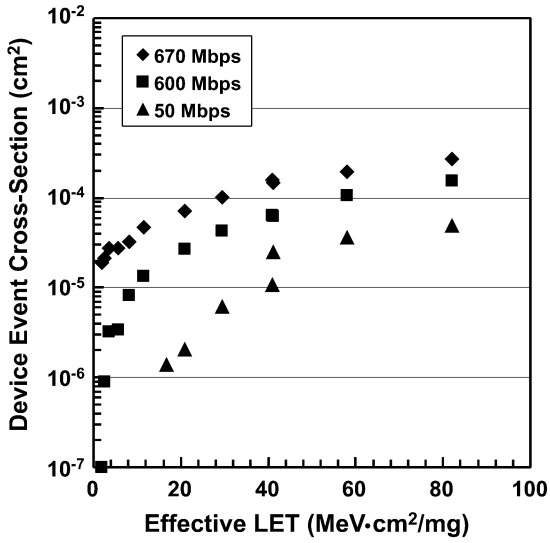


Fig. 10. Trends with data rate for the IBM 5 AM CMOS register show a progression from moderate event sensitivity at 50 Mb/s to increasing cross section and decreasing threshold at 600 Mb/s, and further reduction in threshold and still higher cross section at 670 Mb/s.

cross section of $10^{-4}$ cm$^2$ when the circuit is operated at a data rate of 50 Mb/s. Comparison with the data of Fig. 10 measured at 50, 600, and 670 Mb/s, respectively, shows a pronounced increase in the saturated cross section and a very dramatic reduction in onset LET for the highest data rate of 670 Mb/s. Though not shown, data acquired at 100, 200, and 400 Mb/s are very similar to the 50-Mb/s curve. As with the HBT SiGe counterparts, we note these data are shown as event cross sections. The event cross section trend with data rate for various LETs is shown as Fig. 11(a), and the number of errors per event is shown in Fig. 11(b).

Proton tests of these 5 AM registers were carried out at speed, with no proton upsets noted up to a fluence of $1 \times 10^{12}$ 63 MeV protons at 400 Mb/s. This is consistent with the proton threshold trends seen in Fig. 11. However, at 600 and 670 Mb/s, the proton event cross section exceeded $1 \times 10^{-10}$ cm$^2$, and on average over 5 errors per event were recorded. Unfortunately, the test set used for these tests did not allow full error history capture, but we suspect a similar role of clock tree sensitivity as described for the HBT circuits. We note, in the course of these proton tests, that one part received over 2 Mrad(Si) ionizing dose with no change in supply current, maximum operating frequency, or SEE sensitivity.

## VI. Conclusion

We have long recognized the role of the "window of vulnerability" in high speed CML, ECL, HBT logic families, but these first data showing similar trends in CMOS at only a few hundred megabits per second are remarkable.

The combined heavy ion, proton, and pulsed laser studies reported here describe the SEE characteristics of three important commercially available SiGe related technologies. These studies show significant to extreme SEE sensitivity and represent the first at-speed characterization showing the complex nature of burst-error modes. At speeds achievable with these logic

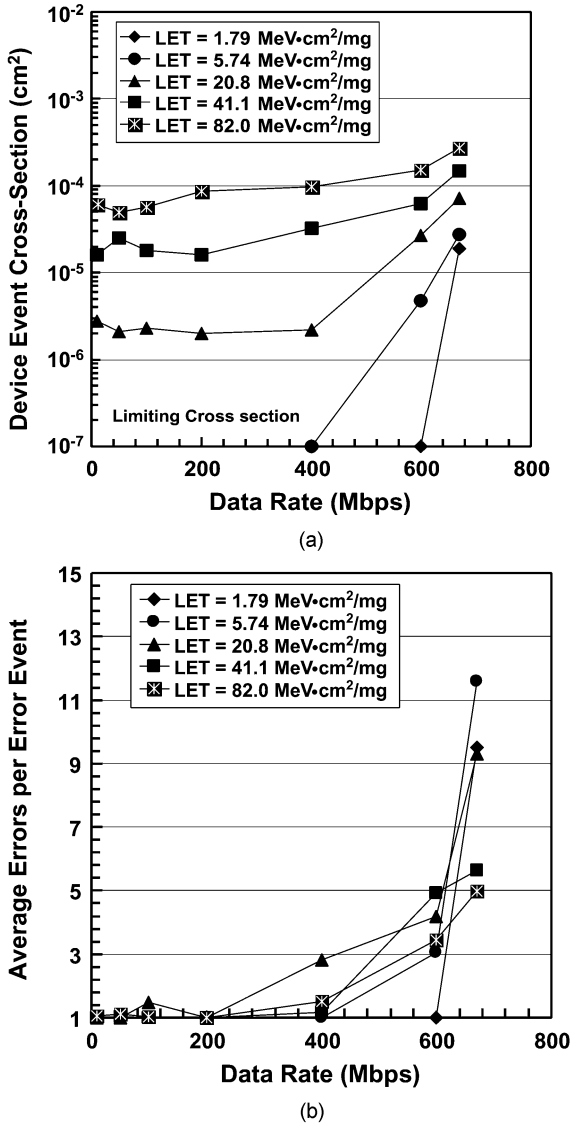


Fig. 11. (a) Data rate dependence of the event cross section for the IBM 5 AM CMOS register at 5 LET values. Significant increases are seen at high data rates, and low LETs become an issue. (b) Average number of errors per event increasing sharply above 400 Mb/s.

families, "single event" should never be confused with "single error" and understanding the true nature of the range of possible errors will be necessary to achieving successful mitigation strategies. The results shown for the HBT logic families are a significant extension of our understanding, not just for these technologies, but for characterization of SEE in high speed technologies in general. Perhaps more importantly, these result seem to apply directly to advanced CMOS circuitry operating at high speeds, and it follows from this study that complex error modes will be characteristic of SEEs in any technology capable of operation with bit periods of shorter duration than the underlying charge collection temporal characteristics, e.g., deep submicron CMOS.

## REFERENCES

[1] J. D. Cressler, "Short Course on Radiation Effects in SiGe HBT BiCMOS Technology," in *Proc. IEEE NSREC*, Monterey, CA, July 21, 2003, pp. V1–V55.

[2] P. W. Marshall, M. A. Carts, A. Campbell, D. McMorrow, S. Buchner, R. Stewart, B. Randall, B. Gilbert, and R. A. Reed, "Single event effects in circuit-hardened SiGe HBT logic at gigabit per second data rates," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2669–2674, Dec. 2000.

[3] R. A. Reed *et al.*, "Heavy-ion broad-beam and microprobe studies of single-event upsets in 0.20 $\mu$m SiGe heterojunction bipolar transistors and circuits," *Trans. Nucl. Sci.*, vol. 50, pp. 2184–2191, Dec. 2003.

[4] G. Niu, R. Krithivasan, J. D. Cressler, P. Marshall, C. Marshall, R. Reed, and D. L. Harame, "Modeling of single-event effects in circuit-hardened high-speed SiGe HBT logic," *IEEE Trans. Nucl. Sci.*, vol. 48, pp. 1849–1854, Dec. 2001.

[5] G. Niu, R. Krithivasan, J. D. Cressler, P. A. Riggs, B. A. Randall, P. W. Marshall, R. A. Reed, and B. Gilbert, "A comparison of SEU tolerance in high-speed SiGe HBT digital logic designed with multiple circuit architectures," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3107–3114, Dec. 2002.

[6] R. Krithivasan, J. D. Cressler, G. Niu, S. M. Currie, K. E. Fritz, P. A. Riggs, B. A. Randall, B. Gilbert, R. A. Reed, and P. W. Marshall, "An SEU hardening approach for high-speed SiGe HBT digital logic," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 2126–2134, Dec. 2003.

[7] G. Niu, J. D. Cressler, M. Shoga, K. Jobe, P. Chu, and D. L. Harame, "Simulation of SEE-induced charge collection in UHV/CVD SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2682–2689, Dec. 2000.

[8] M. Varadharajaperumal, G. Niu, R. Krithivasan, J. D. Cressler, R. A. Reed, P. W. Marshall, G. Vizkelethy, P. E. Dodd, and A. J. Joseph, "3D simulation of heavy-ion induced charge collection in SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2191–2198, Dec. 2003.

[9] D. McMorrow, J. S. Melinger, S. Buchner, T. Scott, R. D. Brown, and N. F. Haddad, "Application of pulsed laser for evaluation and optimization of SEU-hard designs," *IEEE Trans. NucL. Sci.*, vol. 47, pp. 559–565, Dec. 2000.

[10] S. Buchner, K. Kang, D. Krening, G. Lannan, and R. Scheiderwind, "Dependence of the SEU window of vulnerability of a logic circuit on magnitude of deposited charge," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1853–1857, Dec. 1993.

[11] R. A. Reed, M. A. Carts, P. W. Marshall, C. J. Marshall, S. Buchner, M. La Maachia, B. Mathes, and D. McMorrow, "Single event upset cross sections at various data rates," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 2862–2867, Dec. 1996.